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Avalanche Breakdown Diode (ABD) Transient Voltage Suppressors

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AVALANCHE BREAKDOWN DIODE (ABD) TRANSIENT VOLTAGE SUPPRESSORS

Contents

Introduction

Avalanche breakdown diodes (ABDs) described in this document are used as surge protectors by limiting or clamping transient overvoltages and diverting surge currents away from the circuits they are intended to protect. ABDs exhibit relatively high impedance at normal system voltages. They limit transient overvoltages by providing a low impedance to conduct the surge current. These devices may offer either unidirectional or bidirectional protection. ABDs are commonly used in power and communications circuits. Avalanche breakdown diodes are similar to regulator (i.e., Zener) diodes, except that they are designed for short-duration overvoltage protection identified as random recurring transients where cooling occurs before repeating, rather than continuous voltage regulation. They may be single two-lead devices or may have multiple (junctions) devices in a single package.

For the purpose of achieving, specific registration formats are available to fit particular types of avalanche breakdown diodes. These formats are subject to change as new semiconductor developments or circuit applications become practicable. At present, the following formats are available:

NUMBER	DESCRIPTION
RDF-12	Diode, Voltage Transient Suppressor Family

AVALANCHE BREAKDOWN DIODE (ABD) TRANSIENT VOLTAGE SUPPRESSORS
(Device Definitions, Rating Verification Tests, and Characteristic Testing)

(From JEDEC BoD Ballot JCB-04-55 and JCB-12-70, formulated under the cognizance of the JC-22.5 Subcommittee on Transient Voltage Suppressors.)

1 Scope

This standard is applicable to avalanche breakdown diodes when used as a surge protector or transient voltage suppressor (TVS). It describes terms and definitions and explains methods for verifying device ratings and measuring device characteristics. This standard may be applied to other surge-protection components with similar characteristics as the ABD.

2 Terms and definitions

These may use terms similar to other regulator devices such as Zener diodes but have variations unique to ABD's.

2.1 Basic concepts

2.1.1 avalanche breakdown diode (ABD): A transient voltage suppressor that is a semiconductor diode with a single p-n junction (or with multiple p-n junctions none of which interact) whose operation depends in part on its breakdown characteristics.

2.1.2 stand-off (nonconducting) region: The portion of the voltage-current characteristic of a reverse-biased p-n junction that exhibits a high resistance to the passage of current.

2.1.3 breakdown region: The portion of the voltage-current characteristic beyond the initiation of breakdown for an increasing magnitude of reverse current.

2.1.4 forward-conducting region (of a unidirectional ABD): The portion of the voltage-current characteristic of a unidirectional ABD forward-biased p-n junction that exhibits a low small-signal resistance to the passage of current.

2.1.5 anode terminal (A, a): The terminal connected to the p-type region of the p-n junction or, when two or more p-n junctions are connected in series with the same polarity, to the extreme p-type region.

NOTE For unidirectional blocking or low-capacitance ABDs, any rectifier diode(s) that may be included are ignored in the determination of the anode terminal.

2 Terms and definitions (cont'd)

2.1.6 cathode terminal (K, k): The terminal connected to the n-type region of the p-n junction or, when two or more p-n junctions are connected in series with the same polarity, to the extreme n-type region.

NOTE For unidirectional blocking or low-capacitance ABDs, any rectifier diode(s) that may be included are ignored in the determination of the cathode terminal.

2.2 Classes of avalanche breakdown diodes (ABDs)

2.2.1 unidirectional ABD: A two-terminal ABD with a voltage-current avalanche breakdown characteristic in one direction and either a forward or a blocking characteristic in the other. (See Figures 1a and 1b.)

NOTE Large transient currents will be clamped for positive cathode-to-anode voltages when driven into the avalanche breakdown region with one or more p-n junctions placed in series or parallel with each junction connected in the same direction. Large transient currents may also be clamped for negative cathode-to-anode voltages at significantly lower voltages with the typical forward-conducting characteristics of a single p-n junction (or of multiple p-n junctions connected in the same direction). The most common type of unidirectional ABD has a forward-conducting characteristic.

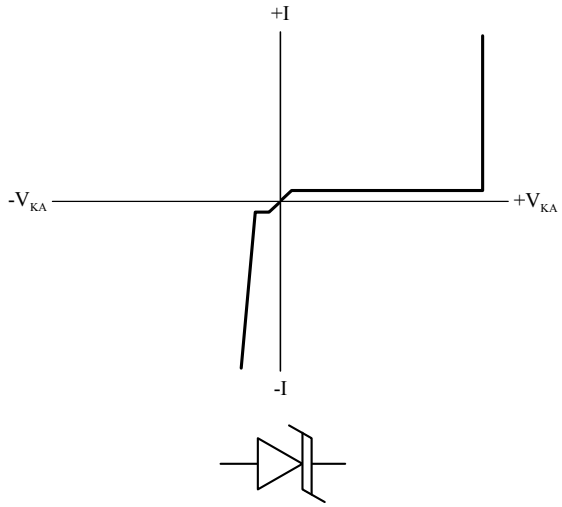


Figure 1a — Unidirectional-conducting ABD

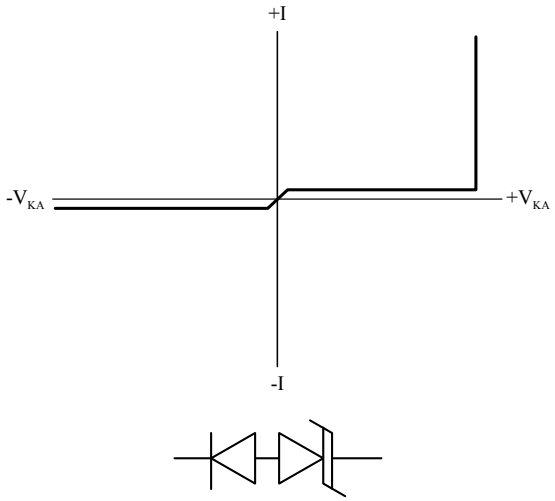


Figure 1b — Unidirectional-blocking ABD

2.2 Classes of avalanche breakdown diodes (ABDs) (cont'd)

2.2.2 bidirectional ABD: A two-terminal ABD with a voltage-current avalanche breakdown characteristic in both directions, which can be either symmetrical (Figure 2a) or asymmetrical (Figure 2b). Figure 2c shows several alternative symbols for the bidirectional ABD.

NOTE Large transient currents will be clamped for voltage of either polarity across two similar p-n junctions in series connected in opposite directions. During a transient current event in this operating mode, one of the two p-n junctions is always in avalanche breakdown and the other is in the forward-conducting, low-voltage mode. The voltage across the bidirectional ABD is the sum of these two voltages. The avalanche breakdown voltage is substantially the same in both directions for a symmetrical bidirectional ABD; however, it may also be intentionally different or asymmetrical by design for special applications. Since multiple p-n junction capacitances in series reduce the overall total capacitance, the bidirectional ABD has lower capacitance than its unidirectional counterpart.

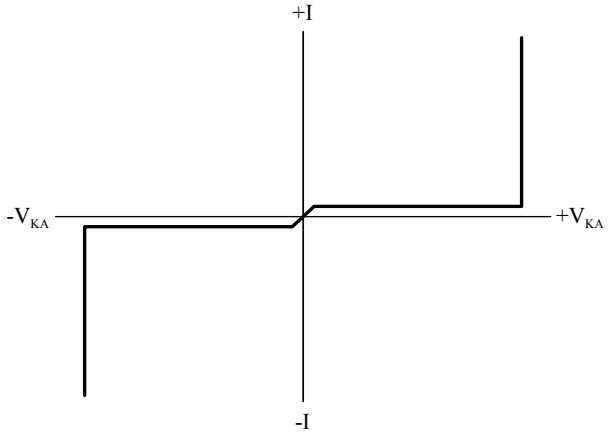


Figure 2a — Symmetrical bidirectional ABD

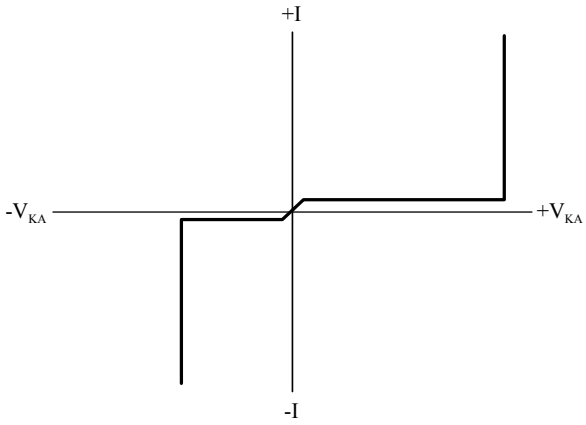


Figure 2b — Asymmetrical bidirectional ABD

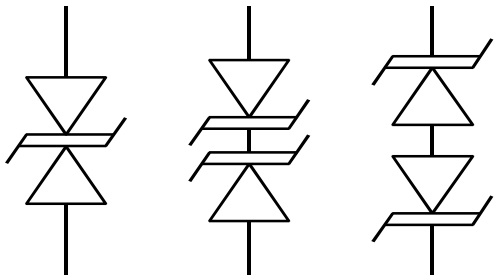


Figure 2c — Bidirectional ABD symbol options

2.2.3 low-capacitance ABD: A two-terminal device that has at least one unidirectional ABD with at least one rectifier p-n junction connected in series with each ABD in the opposite polarity in order to reduce capacitance.

NOTE The rectifier p-n junction(s) operate only in their forward-conducting mode during a transient event.

2.2 Classes of avalanche breakdown diodes (ABDs) (cont'd)

2.2.3.1 unidirectional-blocking low-capacitance ABD: A two-terminal device that has at least one unidirectional ABD with at least one rectifier p-n junction connected in series in the opposite polarity in order to reduce capacitance. (See Figure 3.)

NOTE The unidirectional-blocking low-capacitance ABD is intended to suppress transients in only one direction. The rectifier p-n junction(s) have low capacitance and block in the reverse direction; they are not intended to be operated in their reverse avalanche breakdown regions. The p-n junction that serves as the unidirectional ABD determines which terminal is the anode and which is the cathode; for that determination, the rectifier p-n junction is ignored.

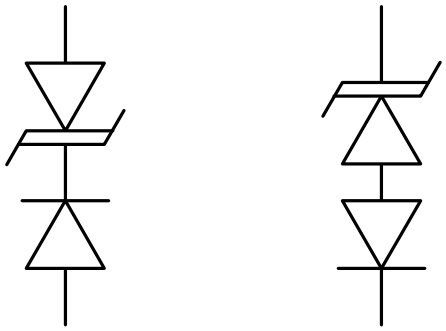


Figure 3 — Unidirectional-blocking low-capacitance ABD

2.2.3.2 unidirectional-conducting low-capacitance ABD: A two-terminal device comprising a unidirectional-blocking low-capacitance ABD and an anti-parallel diode. (See Figure 4.)

NOTE To create a low-capacitance ABD with a forward-conducting, low-voltage characteristic, a low-capacitance diode (such as a rectifier) is placed in anti-parallel to the unidirectional-blocking low-capacitance ABD. This diode must have a reverse blocking voltage greater than the avalanche breakdown voltage of the unidirectional ABD.

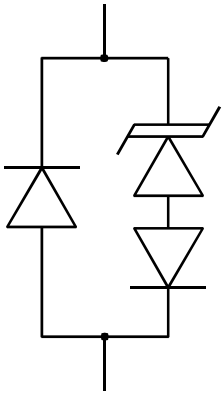


Figure 4 — Unidirectional-conducting low – capacitance ABD

2.2 Classes of avalanche breakdown diodes (ABDs) (cont'd)

2.2.3.3 bidirectional low-capacitance ABD: A two-terminal device comprising two anti-parallel unidirectional-blocking low-capacitance ABD devices. (See Figure 5.)

NOTE The rectifier p-n junctions have low capacitance and must have a reverse blocking voltage greater than the avalanche breakdown voltage of the anti-parallel unidirectional ABD element.

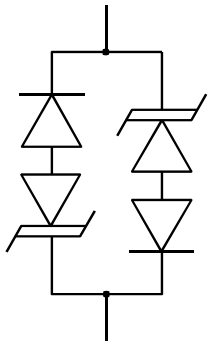


Figure 5 — Bidirectional low-capacitance ABD

2.2.4 ABD array: A device having three or more terminals and containing multiple diodes within a single package, with at least one of the diodes being an ABD.

NOTE ABD arrays can be classified as 1) devices with multiple discrete semiconductor chips; and 2) devices with multiple diode junctions diffused into a single semiconductor chip.

2.3 Avalanche breakdown diode (ABD) specification concepts

2.3.1 Specification concepts for all ABD types

2.3.1.1 rated working standoff voltage (V_{WM}): The maximum-rated value of dc or repetitive peak positive cathode-to-anode voltage that may be continuously applied to an ABD over the standard operating temperature range.

2.3.1.2 standby current (I_D): The current through an ABD at rated stand-off voltage.

2.3.1.3 breakdown [avalanche] voltage ($V_{(BR)}$): The voltage across an ABD at a specified current $I_{(BR)}$ in the breakdown region.

2.3 Avalanche breakdown diode (ABD) specification concepts (cont'd)

2.3.1.4 clamping voltage (V_C or V_{CF}): The voltage across an ABD in a region of low differential resistance that serves to limit the voltage across the device terminals.

NOTE 1 For an asymmetrical device, V_C refers to the clamping voltage in the reverse direction, and V_{CF} refers to the clamping voltage in the forward direction.

NOTE 2 Clamping voltage is measured as the peak voltage across an ABD during the application of an impulse current (I_{PP}) for a specified waveform.

NOTE 3 Due to thermal, reactive, or other effects, peak voltage and peak pulse current may not necessarily be coincident.

2.3.1.5 peak impulse current (I_{PP}): The peak current that is applied to an ABD to determine the clamping voltage (V_C) for a specified impulse waveform.

2.3.1.6 rated random recurring peak impulse current (I_{PPSM}): The maximum-rated value of random recurring peak impulse current that may be applied to a device.

NOTE 1 A repetitive current is usually a function of the circuit and increases the heating effects within the device. A random recurring transient current is usually due to an external cause, and it is assumed that its effect will have completely disappeared before the next transient arrives.

NOTE 2 The symbol I_{PP} or I_{PPM} is often used by the industry; however I_{PPSM} is preferred.

2.3.1.7 rated average power dissipation ($P_{M(AV)}$): The maximum-rated value of power dissipation resulting from all sources, including transients and standby current, averaged over a short period of time.

NOTE This value should be comparable to the dc power rating of the device.

2.3.1.8 rated random recurring peak impulse power dissipation (P_{PPSM}): The maximum-rated value of the product of rated random recurring peak impulse current (I_{PPSM}) and specified maximum clamping voltage (V_C).

NOTE 1 A repetitive peak impulse power is usually a function of the circuit and increases the heating effects within the device. A random recurring transient peak impulse power is usually due to an external cause, and it is assumed that its effect will have completely disappeared before the next transient arrives.

NOTE 2 The symbol P_{PP} or P_{PPM} is often used by the industry; however P_{PPSM} is preferred.

2.3 Avalanche breakdown diode (ABD) specification concepts (cont'd)

2.3.1.9 peak overshoot voltage (V_{OS}): The excess voltage above the clamping voltage (V_C) of a device for a given test waveform that occurs when waveshapes having a virtual front time of less than 10 µs are applied.

NOTE This value may be expressed as a percentage of the clamping voltage. It is dependent on the lead inductance of the device and the fast front time of the test waveform.

2.3.1.10 incremental surge resistance (R_S): The difference between two instantaneous values of the clamping voltage, divided by the difference between the corresponding values of the peak impulse current.

$$R_S = \frac{V_{C2} - V_{C1}}{I_{PP2} - I_{PP1}}$$

NOTE This resistance is composed of thermal and nonlinear avalanche components.

2.3.1.11 peak ESD limiting voltage (V_P): The peak voltage resulting from a fast-front-time waveform, such as electrostatic discharge (ESD).

2.3.1.12 (standard) impulse waveshape: A waveform that has a defined virtual front time and a defined virtual time to half peak value.

NOTE 1 Impulse waveshapes may be given for either voltage or current. See Figures 6a and 6b for examples.

NOTE 2 Virtual front time is the time interval between the virtual origin and the instant when the extrapolated leading edge reaches its peak; the extrapolation is made through the 10% and 90% amplitude points for current and the 30% and 90% points for voltage.

NOTE 3 Virtual time to half-peak value is the time interval between the virtual origin and the instant when the amplitude of the trailing edge reaches 50%. This is expressed as a combined front time and time to half-peak value such as 8/20 µs or 10/1000 µs.

2.3 Avalanche breakdown diode (ABD) specification concepts (cont'd)

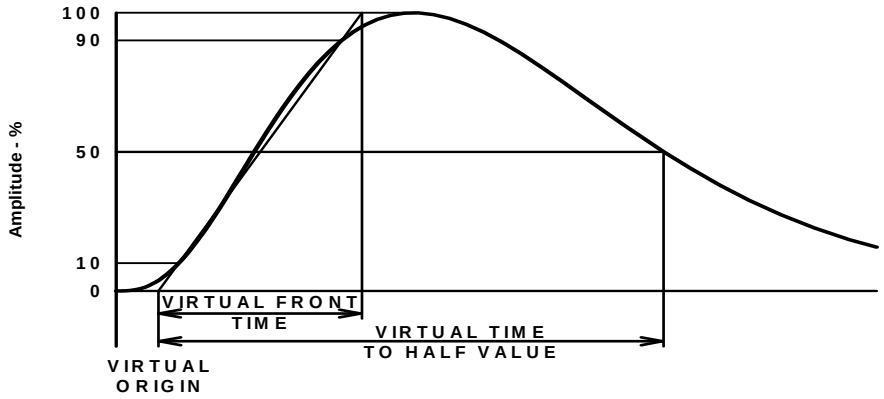


Figure 6a — Standard current impulse waveshape

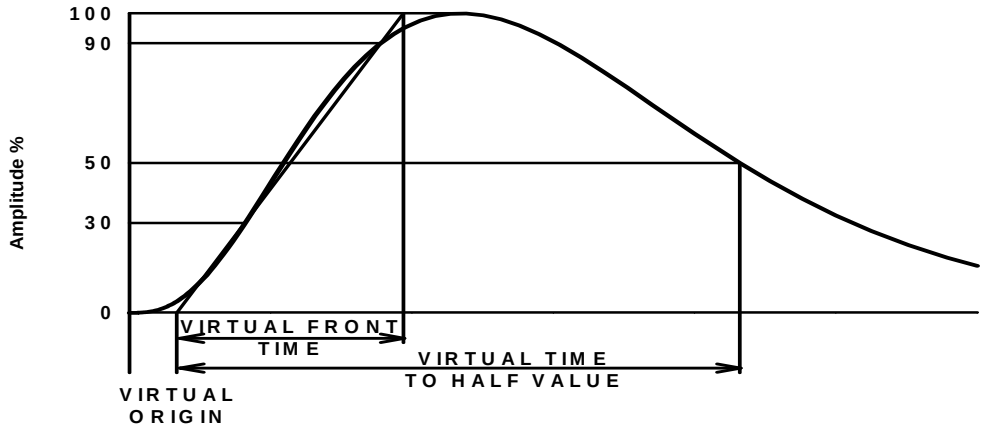


Figure 6b — Standard voltage impulse waveshape

2.3.2 Thermal specification concepts for all ABD types

2.3.2.1 temperature coefficient of breakdown voltage ($\alpha_{V(BR)}$): The change in breakdown voltage divided by the change in temperature.

NOTE This quotient may be expressed as mV/°C, mV/K, %/°C, or %/K.

2.3 Avalanche breakdown diode (ABD) specification concepts (cont'd)

2.3.2.2 temperature derating: A specification showing how a rating stated at a particular temperature is reduced at higher temperatures.

NOTE 1 Derating is usually expressed graphically or in terms of derating factors (e.g., mA/°C or mW/°C). When shown graphically, ABD curves are often shown as a percentage of the maximum or peak value derating from 100% down to 0%.

NOTE 2 For ABDs, derating applies to ratings for peak pulse current (I_{PPSM}), peak pulse power (P_{PPSM}), and steady-state (average power) dissipation ($P_{M(AV)}$).

NOTE 3 Steady-state (average) power ratings derate from 100% to zero at the maximum junction temperature rating (T_{JM}). Transients operating at peak ratings can cause the junction temperature to exceed T_{JM} for limited time durations, without damage to the device. As a result, peak pulse ratings derate at a slower rate than steady-state ratings. However, the continuous elevated base temperature for peak ratings may not exceed T_{JM} and the derated value must be zero at T_{JM}.

NOTE 4 The average power-derating curve is derived from $P_{M(AV)} = (T_{JM} - T_X)/ R_{\theta JX}$, where the subscript "X" can indicate L (for lead), C (for case) or A (for ambient). The average power-derating curve is drawn with a slope of $-1/R_{\theta JX}$ from 0% at $T_X = T_{JM}$ up to 100% at a value of temperature equal to or above 25 °C, but below T_{JM}. .

NOTE 5 The rectangular-wave peak power-derating curve is derived from $P_{PPSM} = (T_{JP} - T_X)/ Z_{\theta JX}$, where the subscript "X" can indicate L (for lead), C (for case) or A (for ambient). TJP is the peak junction temperature that the ABD can withstand for the limited time duration of the transient impulse, and $Z_{\theta JX}$ is the thermal impedance for that same transient time interval. The peak power-derating curve is drawn derating from the peak value of P_{PPSM} at $T_X = 25$ °C down with a slope of $-1/Z_{\theta JX}$ to whatever the value is at $T_X = T_{JM}$. Then the curve goes vertically down to 0% at $T_X = T_{JM}$. Other waveforms will require different correction factors for the calculation of P_{PPSM}.

NOTE 6 A typical derating curve for P_{PPSM} and $P_{M(AV)}$ is shown in Figure 7.

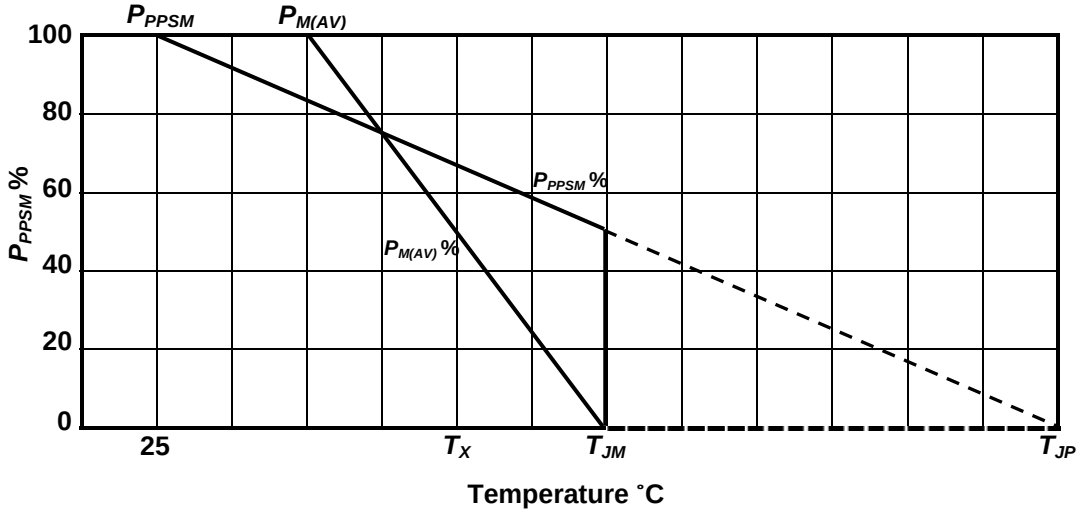


Figure 7 — ABD Derating Curve

2.3 Avalanche breakdown diode (ABD) specification concepts (cont'd)

2.3.2.3 thermal resistance, junction-to-ambient [junction-to-case] [junction-to-lead] ($R_{\theta JA}$ or R_{thJA}; $R_{\theta JC}$ or R_{thJC}; $R_{\theta JL}$ or R_{thJL}): The temperature difference between two specified points or regions divided by the power dissipation, under conditions of thermal equilibrium.

2.3.2.4 thermal impedance, (transient), junction-to-ambient [junction-to-case] [junction-to-lead] ($Z_{\theta JA}$ or Z_{thJA}, $Z_{\theta JC}$ or Z_{thJC}, $Z_{\theta JL}$ or Z_{thJL}): The change in temperature difference between two specified points or regions that occurs during a time interval divided by the step-function change in power dissipation that occurred at the beginning of the interval and caused the change in temperature difference.

2.3.3 Additional specification concepts for unidirectional-conducting ABD devices

2.3.3.1 peak forward surge voltage (V_{FS}): The peak voltage across an ABD for a specified forward surge current (I_{FS}) and time duration.

2.3.3.2 forward surge current (I_{FS}): A pulsed current through an ABD in the forward conducting region.

2.3.3.3 rated forward surge current (I_{FSM}): The maximum-rated value of peak forward current that may be applied as a single 8.3-ms or 10-ms half-sine-wave pulse.

2.3.4 Additional specification concepts for low-capacitance ABD devices

2.3.4.1 capacitance (C or C_J): The capacitance between the two terminals of an ABD.

2.3.4.2 insertion loss: The ratio of power delivered to a load with no ABD in the circuit to that delivered after the ABD is inserted.

NOTE Insertion loss is generally expressed in decibels. It is frequency-dependent due to the inductance, capacitance, and resistance of the ABD.

2.3 Avalanche breakdown diode (ABD) specification concepts (cont'd)

2.3.5 Additional specification concepts for ABD arrays

2.3.5.1 cross-talk voltage (V_{CT}): The incremental voltage across the terminals of one ABD resulting from an electrical pulse in an adjacent ABD within a single array package.

2.3.5.2 simultaneous surge: An impulse current pulse applied simultaneously to multiple terminals of a single-chip ABD array.

NOTE A simultaneous surge test may be used to determine the worst-case impulse current through an array of p-n junction ABDs having a common chip connection where current crowding may cause a failure or degradation of the device.

2.3.6 Additional specification concepts for unidirectional-blocking low-capacitance ABD devices

2.3.6.1 blocking leakage current (I_{IB}): The current through a unidirectional-blocking low-capacitance ABD at rated inverse blocking voltage (V_{WIB}).

2.3.6.2 rated inverse blocking voltage (V_{WIB}): The maximum-rated value of dc or peak blocking voltage that may be applied to a unidirectional-blocking low-capacitance ABD in the inverse direction.

NOTE Above this rated voltage, the ABD is not to be surge or impulse tested for any reason.

3 Rating verification tests

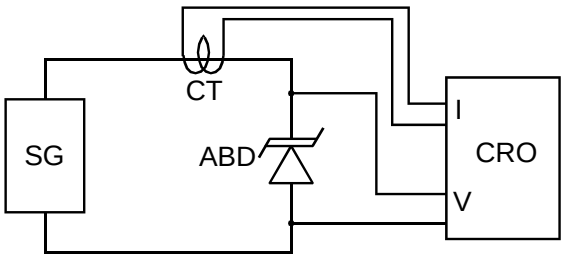
All tests are to be at 25 °C unless otherwise specified

3.1 Rated random recurring peak Impulse power dissipation (P_{PPSM})

The purpose of this test is to verify the peak impulse pulse power rating under a specified set of test conditions. Verification requires the application of the rated random recurring peak impulse current (I_{PPSM}) and measuring the clamping voltage (V_C) with a circuit functionally equivalent to Figure 7. Multiplication of the peak impulse current by the clamping voltage is defined as the peak impulse power dissipation. A sufficient number of devices shall be tested to obtain a statistical distribution within the desired confidence limits.

NOTE For this test, two waveshapes are recommended, 8/20 μs and 10/1000 μs, for purpose of obtaining consistent data on similar ABD devices.

3.1 Rated random recurring peak Impulse power dissipation (P_{PPSM})



SG = Transient (surge) Generator
CT = Current Transformer or equivalent
CRO = Oscilloscope for measuring peak Current and peak Voltage

NOTE Peak Impulse Power is the peak current times the peak voltage (current and voltage may not be coincident in time).

Figure 8 — Peak impulse power test circuit

3.1.1 Test conditions to be specified

a. Ambient (T_A), case (T_C), or lead (T_L) temperature = ____ ^{o}C

b. Peak impulse current (I_{PPSM}) = ____ A

c. Waveshape (Impulse) = ___ / ___ µs

3.1.2 Parameter to be measured

a. Peak Clamping Voltage (V_C) = ____ V

3.1.3 Parameter to be calculated

a. Peak Impulse Power (P_{PPSM}) = I_{PPSM} x V_C = ____W

3.2 Rated average power dissipation ($P_{M(AV)}$)

The rated average power dissipation test is to verify the repetitive current transient condition for a specified duty factor. Depending upon the device packaging, the ABD will have a defined thermal resistance from junction to the case, lead, or ambient air that is used to specify the average power dissipation. The peak pulse power times the duty factor of the current pulse square wave must be less than the rated average power dissipation. The transient test generator shall be specified for the short current pulse values and the duty factor. The test circuit used shall also be functionally equivalent to Figure 8.

NOTE Duty factor (DF) = 100 t_p/t_{rep}, expressed in percent, where t_{rep} is the pulse period.

3.2 Rated average power dissipation ($P_{M(AV)}$) (cont'd)

3.2.1 Test condition to be specified

a. Ambient (T_A), case (T_C), or lead (T_L) temperature = ____ °C

b. Peak Current (I_T) = _____A

c. Pulse width (t_P) = _____s

d. Period (t_{rep}) = _____ s

3.2.2 Parameter to be measured

a. Peak Voltage (V_P) = _____V

3.2.3 Parameter to be calculated

a. Average power dissipation ($P_{M(AV)}$) = _____W
$[V_P \times I_T \times t_p / t_{rep}]$

3.3 Rated random recurring peak impulse current (I_{PPSM})

The rated random recurring peak impulse current test is to verify that the ABD can withstand a number of current impulses of the same peak value without causing failure. After the number of impulses are applied, the standby current (I_D) shall be within specification (see 4.2).

3.4 Rated forward surge current (I_{FSM})

The rated forward surge current test is to verify that the ABD can withstand the maximum peak current for an 8.3-ms or 10-ms half-sine-wave nonrepetive pulse without causing device failure. This test applies to unidirectional ABDs only. After the pulse has been applied, the standby current (I_D) shall be within specification (see 4.2).

3.4.1 Test conditions to be specified

a. Ambient (T_A), case (T_C), or lead (T_L) temperature = ____ °C

b. Peak impulse current (I_{FSM}) = ____ A

c. Waveshape = ___ / ____ ms

3.4.2 Parameter to be measured - Optional

a. Peak Clamping Voltage (V_{FS}) = ____ V

3.5 Rated working standoff voltage (V_{WM})

The working standoff voltage test is to verify that the ABD can withstand rated dc voltage without causing device failure. After the voltage has been applied the standby current (I_D) shall be within specification (see 4.2).

4 Characteristic tests

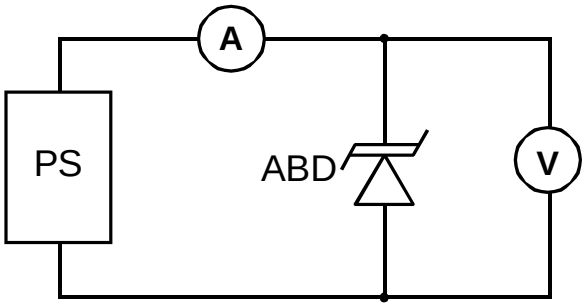
All tests are to be done at 25 ^oC unless otherwise specified

4.1 Breakdown (avalanche) voltage ($V_{(BR)}$)

The purpose of this test is to determine the breakdown (avalanche) voltage of the ABD at a specified pulsed dc current.

4.1.1 Procedure

The test generator shall be a low-current, less than 25 mA, constant-current source or equivalent. An oscilloscope shall be used to measure the voltage across the ABD. For bidirectional devices, each polarity is to be tested by reversing the test generator polarity. The test circuit shall be functionally equivalent to Figure 9. A pulse of specified width and breakdown current, $I_{(BR)}$, amplitude shall be applied to the ABD and the stabilized value of breakdown voltage, $V_{(BR)}$, measured near the pulse end using a circuit functionally equivalent to Figure 8. In the absence of special requirements, it is recommended that the pulse width be less than 400 ms with a test current, $I_{(BR)}$, of 1 mA. Each polarity of the ABD must be separately tested and measured. The value of $V_{(BR)}$ is junction-temperature (initial and increase due to testing) and test-current dependent. Pulse testing minimizes these thermal effects.



PS = Power Supply A = Ammeter (mA) V = Voltmeter

Figure 9 — Breakdown voltage test circuit

4.1 Breakdown (avalanche) voltage ($V_{(BR)}$) (cont'd)

4.1.2 Test conditions to be specified

a. Ambient (T_A), case (T_C), or lead (T_L) temperature = _____ ^{o}C

b. Breakdown current ($I_{(BR)}$) =_____ mA

c. Breakdown current pulse width =_____ μs

4.1.3 Characteristics to be measured

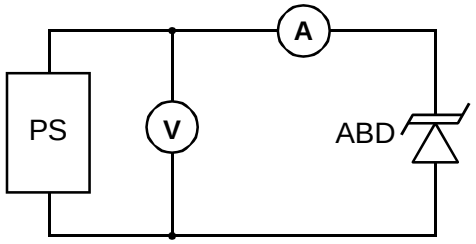
a. Breakdown (avalanche) Voltage ($V_{(BR)}$) = _____ V

4.2 Standby current (I_D) or blocking leakage current (I_{IB})

The purpose of this test is to determine the standby current [or blocking leakage current] of the ABD at rated stand-off voltage [or rated inverse blocking voltage] and specified temperature.

4.2.1 Procedure

The rated stand-off voltage [or rated inverse blocking voltage] shall be generated from a well-regulated dc power supply. The resultant dc current shall be measured with an ammeter. The current shall be applied for at least 10 ms to allow stabilization of the conduction. The test circuit used shall be functionally equivalent to Figure 10.



A = Ammeter V = Voltmeter PS = DC power supply set to V_D

Figure 10 — Standby or blocking leakage current test circuit

4.2.2 Test conditions to be specified

a. Ambient (T_A), case (T_C), or lead (T_L) temperature = _____°C

b. DC standoff voltage (V_{WM}) [or inverse blocking voltage (V_{WIB})] = _____ V

4.2 Standby current (I_D) or blocking leakage current (I_{IB}) (cont'd)

4.2.3 Characteristics to be measured

a. Standby current (I_D) [or blocking leakage current (I_{IB})] = _____ µA

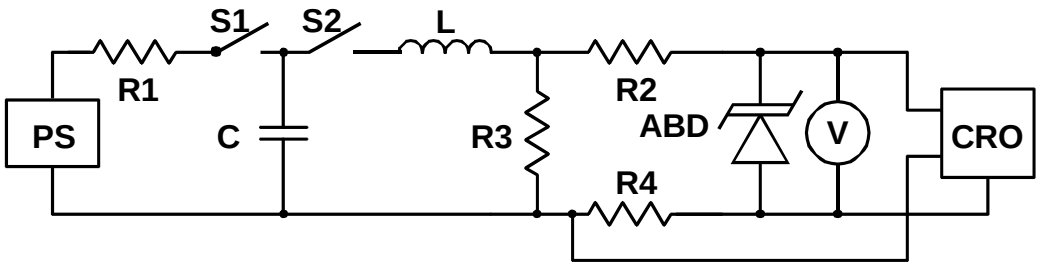
4.3 Clamping voltage (V_C)

The purpose of this test is to determine the peak clamping voltage in the breakdown region, when the ABD is conducting a current impulse (I_{PP}) of a specified waveshape.

4.3.1 Procedure

The device under test is connected to a surge generator and the resultant peak clamping voltage is measured with a digital voltmeter or oscilloscope. The test circuit used shall be functionally equivalent to Figure 11. Typically waveshapes used for ABD device characterizations are 8/20 µs or 10/1000 µs.

Bidirectional devices require a test for each polarity. However, sufficient time must be allowed between the testing of each polarity to allow junction cooling.



PS = Charging Power Supply
S1 = Charging Switch
S2 = Impulse Discharge Switch
R3 = Impulse Shaping Resistor
R4 = Current Sensing Resistor
R1 = Charging Resistor
C = Impulse Shaping Capacitor
L = Impulse Shaping inductor
R2 = Impulse Shaping and Current Limiting Resistor
V = Peak reading Voltmeter
CRO = Oscilloscope for observing Current and Voltage

CAUTION The circuit shown is for description only. Measurement techniques for high current, high frequency testing should be observed, such as four point Kelvin contact, differential oscilloscope, short leads etc.

NOTE The power supply and the charging and shaping components (R1 / C, S1, S2, L / R3) of the circuit can be replaced by a transient generator.

Figure 11 — Clamping voltage test circuit

4.3 Clamping voltage (V_C) (cont'd)

4.3.2 Test conditions to be specified

a. Ambient (T_A), case (T_C), or lead (T_L) temperature = _____ °C

b. Peak Pulse Current (I_{PP}) = _____ A

c. Waveshape = _____ /_____ µs

4.3.3 Characteristics to be measured

a. Clamping voltage (V_C) = _____ V

4.4 Forward surge voltage (V_{FS})

The purpose of this test is to measure the peak forward voltage of a unidirectional conducting ABD at a specified forward surge current (I_{FS}).

4.4.1 Procedure

A pulsed forward current is applied to the ABD and the resultant voltage is measured. This applies to an ABD that is defined as forward conducting and a unidirectional conducting low capacitance ABD.

4.4.2 Test conditions to be specified

a. Ambient (T_A), case (T_C), or lead (T_L) temperature = _____°C

b. Pulsed forward surge current (I_{FS}) = ____ A

c. Waveshape

1. Impulse (Double exponential) = ____/ ____ µs
2. ½ Sinewave = _____ ms
3. Squarewave =_____ ms

4.4.2 Characteristics to be measured

a. Forward voltage (V_F) = _____ V

4.5 Capacitance (*C* or C_J)

The purpose of this test is to determine the junction capacitance of an ABD between any two terminals at a specified sinusoidal frequency and bias voltage. For multiple terminal devices, one pair of terminals shall be measured at a time; all terminals not involved in the test shall be guarded to remove their capacitance from the measurement.

4.5.1 Procedure

The capacitance shall be measured at a dc bias voltage (V_{WM}) and ac signal voltage for a specified frequency. If the capacitance measuring equipment does not have a built in signal voltage, then use an ac rms voltage of 0.1 V between the frequencies of 100 kHz and 1 MHz. The test circuit shall be functionally equivalent to Figure 12.

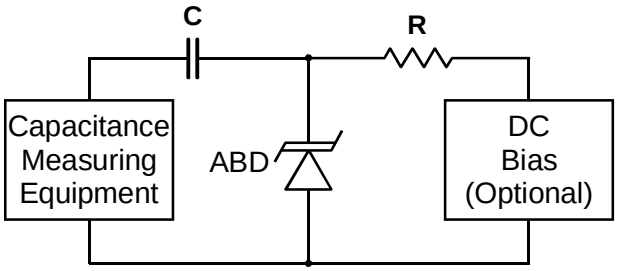


Figure 12 — Capacitance test circuit

4.5.2 Test conditions to be specified

a. DC bias voltage = _____ V

b. Frequency = _____ ___Hz

c. AC rms signal voltage =_____ V

4.5.3 Characteristics to be measured

a. Capacitance (C_J) = _____ pF

4.6 Temperature coefficient of breakdown voltage ($\alpha_{V(BR)}$)

The purpose of this test is to determine the rate of change of breakdown voltage, $V_{(BR)}$, between two specified temperatures. (See MIL-STD-750 method 4071)

4.6.1 Procedure

The breakdown voltage shall be measured as described 4.1, Breakdown (avalanche) Voltage ($V_{(BR)}$), with a pulse of specified width, (t_W) and breakdown current, ($I_{(BR)}$), at the reference temperature (T_{REF}) and a second test temperatures (T_{TEST}). Thermal equilibrium shall be established at each measurement temperature before the breakdown voltage is measured. In cases where the ADB is not symmetrical in construction or voltage or both, each breakdown polarity of the ADB must be separately measured.

4.6.2 Test conditions to be specified

a. Reference temperature (T_{REF}) = _____ ^{o}C

b. Test temperature (T_{TEST}) = _____ ^{o}C

c. Temperature reference measurement point (Ambient, case or lead) = _____

d. Breakdown current ($I_{(BR)}$) =_____ mA

e. Breakdown current pulse width (t_W) =_____ μs

4.6.3 Characteristics to be measured

a. Breakdown (avalanche) Voltage ($V_{(BR)REF}$) = _____ V

b. Breakdown (avalanche) Voltage ($V_{(BR)TEST}$) = _____ V

4.6.4 Calculation

The temperature coefficient can be expressed as either the average %/K or mV/K change over the specified temperature range.

$\alpha_{V(BR)} = 1000(V_{(BR)TEST} - V_{(BR)REF})/(T_{TEST} - T_{REF})$ mV/K

or

$\alpha_{V(BR)} = 100(V_{(BR)TEST} - V_{(BR)REF})/((T_{TEST} - T_{REF})(V_{(BR)REF}))$ %/K

4.7 Thermal impedance ($Z_{\theta JA}$ or Z_{thJA}, $Z_{\theta JC}$ or Z_{thJC}, $Z_{\theta JL}$ or Z_{thJL})

The purpose of this test is to determine the power capability of an ABD, for a specified heating power pulse duration at a given reference temperature. The transient thermal impedance of a semiconductor device is a measure of the ability of its mechanical structure to provide for heat storage as well as heat removal from the active semiconductor element (See Mil-Std-750 method 3100)

One dimension heat flow is assumed in transient thermal impedance specifications and such specifications must always include the two points or planes between which the thermal resistance or transient thermal impedance value applies. The term virtual junction temperature is here applied to indicate the temperature of the active semiconductor element for use in the device test methods and specifications. The reference (R) temperature is usually established at one of the following:

a) The ambient air (A).

b) A specified point on the case (C)

c) A specified point on a lead (L)

4.7.1 Equations and letter symbols

Transient thermal impedance is defined as:

$$Z_{\theta JR(t)} = (T_{J(t)} - T_R) / P_{(BR)(AV)}$$
$$= 1000K(V_{(BR)(MET)1} - V_{(BR)(MET)3}) / (V_{(BR)(HTG)(AV)} \times I_{(BR)(HTG)})$$

where:

$I_{(BR)(HTG)}$ – Heating current used to produce the power dissipated in the ABD.

K – Thermal Calibration Factor = $\Delta T_{(CAL)} / \Delta V_{(BR)(MET)}$ K/mV

where:

$\Delta T_{(CAL)}$ – Difference between two calibration temperatures, T_{JMAX} and T_R, applied to the reference point.

$\Delta V_{(BR)(MET)}$ – Difference in $V_{(BR)(MET)}$ when measured at two calibration temperatures, T_R and T_{JMAX}, in millivolts.

$V_{(BR)(MET)}$ – Value of breakdown voltage at $I_{(BR)(MET)}$, the TSP.

$I_{(BR)(MET)}$ – Value of metering current, in milliamperes.

T_{JMAX} – Maximum rated junction temperature

$P_{(BR)(AV)}$ – Magnitude of average heating power causing temperature difference $T_{J(t)} - T_R$.

$V_{(BR)(HTG)(AV)}$ – Average measured value of breakdown voltage for the period when $I_{(BR)(HTG)}$ is applied.

4.7.1 Equations and letter symbols (cont'd)

$V_{(BR)(MET)1}$ – Value of the TSP at the reference temperature used in the test procedure.
$V_{(BR)(MET)3}$ – Value of the TSP immediately after the $I_{(BR)(HTG)}$ pulse is terminated.
$T_{J(t)}$ – Measured junction temperature at time t.
T_R – Measured reference (case, lead, or ambient) temperature
TSP – Temperature-sensitive parameter.

NOTE In this procedure the temperature-sensitive parameter (TSP) is $V_{(BR)}$. Forward voltage, V_F, may also be used for a unidirectional ABD.

$Z_{\theta JR(t)}$ – Transient thermal impedance at a given time, junction to reference point, in Kelvin/Watt.

Other letter symbols used are:
$R_{\theta JR}$ – Thermal resistance, junction to reference point, in Kelvin/Watt.

NOTE This is the value of $Z_{\theta t)}$ for steady state conditions when time does not affect the value

T_{R2} – Measured reference (case, lead, or ambient) temperature when operated with power applied.

4.7.2 Procedure

There are two steps in the procedure: TSP calibration and measurement under power pulse conditions.

TSP ($V_{(BR)}$) calibration uses the breakdown (avalanche) voltage ($V_{(BR)}$) test circuit and a similar testing procedure to temperature coefficient of breakdown voltage ($\alpha_{V(BR)}$). K is the reciprocal of $\alpha_{V(BR)}$.

Calibration consists of operating the test device at a metering current that causes no significant power dissipation, so that for all practical purposes, the ABD virtual junction temperature and the reference temperature will be equal. This value of metering current, $I_{(BR)(MET)}$ shall used in the power pulse testing.

First, the ABD TSP is measured at the reference temperature, T_R, to be used for the power pulse testing. The TSP voltage is monitored while the ABD is externally heated on a temperature-controlled block or in an oven to the ABD maximum rated junction temperature, T_{JMAX}. When the TSP voltage has stabilized its value is measured.

In some cases, there may be significant device-to-device variation of the TSP, which could cause unacceptable $Z_{\theta JR}$ inaccuracies. Either each device shall be individually calibrated or statistical techniques shall be used to guarantee the maximum value of $Z_{\theta JR}$.

4.7.2 Procedure (cont'd)

The heating power pulse test circuit used shall be functionally equivalent to Figure 13. Power pulse testing applies two currents: one for TSP measurement, $\boldsymbol{I_{(BR)(MET)}}$ from PS2 with switch in position shown, and the other for heating, $\boldsymbol{I_{(BR)(HTG)}}$ from PS1 with switch operated for time t. Voltage measurements of $\boldsymbol{V_{(BR)}}$, are taken immediately prior, during and immediately after the heating power pulse. At the same time $\boldsymbol{I_{(BR)}}$ verification measurements are taken of $\boldsymbol{I_{(BR)(MET)}}$ and $\boldsymbol{I_{(BR)(HTG)}}$ in the ABD. In cases where the ABD is not symmetrical in construction or voltage or both, each breakdown polarity of the ABD must be separately measured.

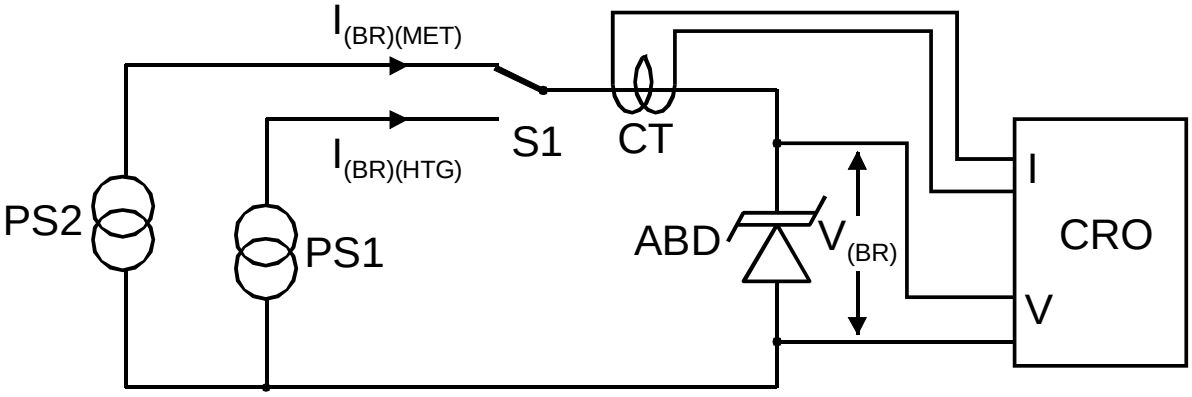


Figure 13 — Thermal impedance test circuit

The heating current is applied as a single pulse approximately rectangular in shape and of specified width, corresponding to the time value for which the transient thermal impedance is to be measured. If the heating current waveform deviates much from a truly rectangular pulse, then graphical integration of the product of the heating current and heating voltage waveforms must be employed to determine the ABD power dissipation. Care must be taken, when applying heating current pulses, to avoid exceeding device random recurring surge current capabilities.

If the temperature after the power pulse is not within +0 % -20 % of the device maximum junction temperature, $\boldsymbol{T_{JMAX}}$, the test shall be repeated with the heating pulse current amplitude appropriately adjusted until the required temperature is achieved. Adequate time shall be allowed between tests for the device to regain thermal equilibrium. Since the transient thermal impedance is lower for short pulse widths than for long pulse widths, a higher amplitude current pulse is required to heat the device junction when the pulse width is short.

For all but very short pulse widths it is generally necessary to employ an external heat dissipator to prevent appreciable device case or lead reference temperature rise during the interval when power is applied. For pulses longer than 50 ms, the reference temperature may increase and the calculated $Z_{\theta JR}$ will be higher than the true value. The $Z_{\theta JR}$ value may be corrected by using the actual reference temperature value, T_{R2}, at the end of the test.

4.7.2 Procedure (cont'd)

When an approximate value for the test device transient thermal impedance is known, the $Z_{\theta JR}$ equation may be employed to calculate the approximate value of heating current required to raise the device virtual junction temperature to maximum rated value; otherwise, the required current magnitude must be arrived at by trial and error.

After the heating pulse, switching transients may prevent an accurate TSP reading until time t_3, see Figure 14. During this time the junction temperature cools and so the calculated $\boldsymbol{T_J}$ temperature will be low. This temperature error can be corrected by taking successive measurements after the heating pulse at t_3 and t_4, then linearly extrapolating the temperature decay back to the time, t_1, when the pulse ended.

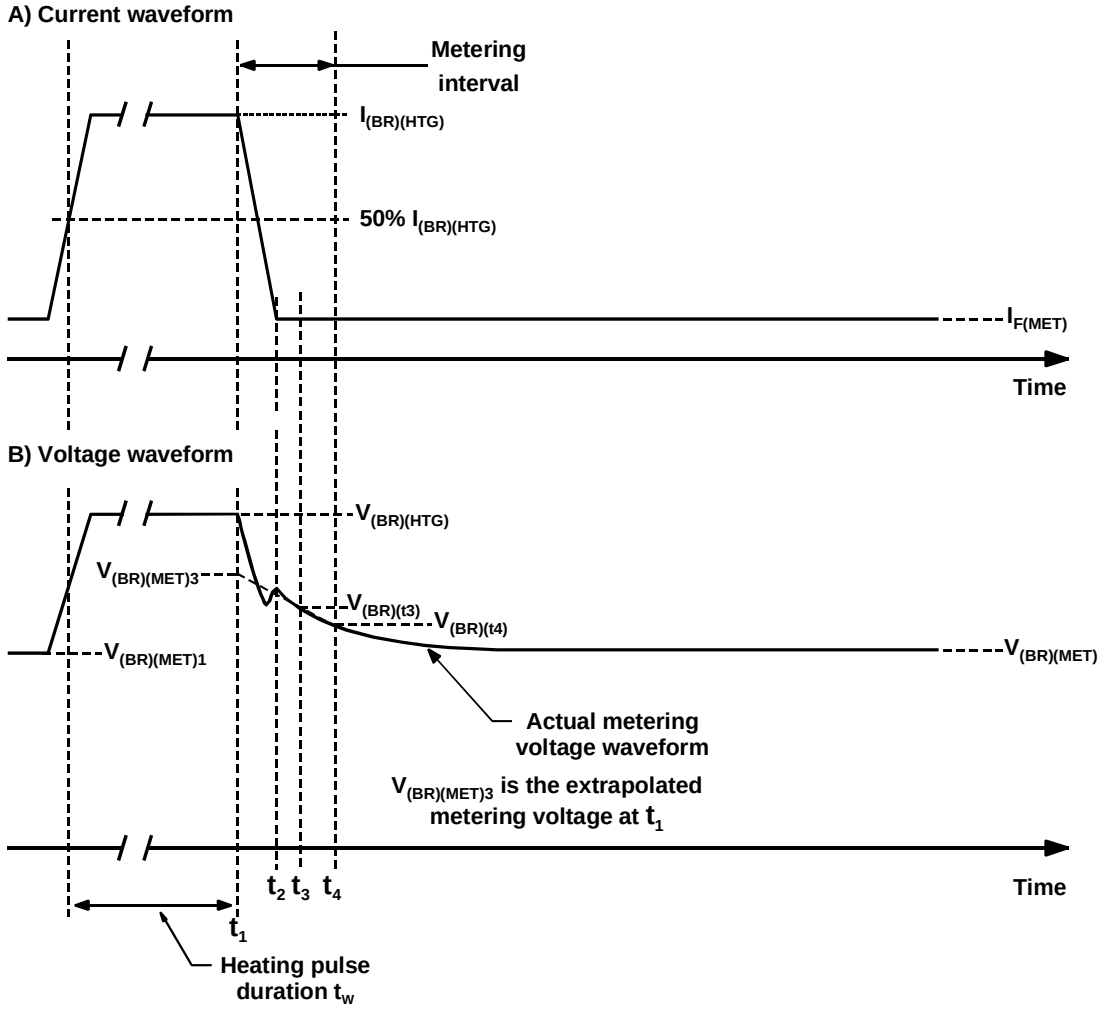


Figure 14 — Thermal impedance waveshapes

In the absence of special requirements, it is recommended that the value of $Z_{\text{th(t)}}$ be determined over a time interval of 100 µs to a time duration approximating steady state operation and expressed as a graph.

4.7.3 Test conditions to be specified

a. Reference temperature (T_R) = _____ °C

b. Maximum junction temperature (T_{JMAX}) = _____ °C

c. Temperature reference measurement point (Ambient, case or lead) = _____ °C

d. TSP (breakdown) metering current ($I_{(BR)(MET)}$) =_____ mA

e. ABD heating current ($I_{(BR)(HTG)}$) =_____ A

f. Heating current pulse width (t_W) =_____ ms

g. Measurement time t_3 for $V_{(BR)(t3)}$ =_____ ms

h. Measurement time t_4 for $V_{(BR)(t4)}$ =_____ ms

4.7.4 Characteristics to be measured

a. TSP (breakdown) metering voltage ($V_{(BR)(MET)1}$) at T_R =_____ V

b. TSP (breakdown) metering voltage ($V_{(BR)(MET)2}$) at T_{JMAX} =_____ V

c. TSP (breakdown) metering voltage ($V_{(BR)(t3)}$) at t_3 =_____ V

d. TSP (breakdown) metering voltage ($V_{(BR)(t4)}$) at t_4 =_____ V

e. ABD average heating voltage ($V_{(BR)(HTG)(AV)}$) = _____ V

4.7.5 Calculation

The temperature coefficient can be expressed as either the average %/K or mV/K change over the specified temperature range.

$K = (T_{JMAX} - T_R)/(V_{(BR)(MET)2} - V_{(BR)(MET)1})$ K/mV

$V_{(BR)(MET)2}$ by extrapolation using $V_{(BR)(t3)}$ at t_3 and $V_{(BR)(t4)}$ at t_4

$Z_{\theta JR(t)} = 1000K(V_{(BR)(MET)1} - V_{(BR)(MET)3}) / (V_{(BR)(HTG)(AV)} \times I_{(BR)(HTG)})$

4.8 Thermal resistance ($R_{\theta JA}$ or R_{thJA}; $R_{\theta JC}$ or R_{thJC}; $R_{\theta JL}$ or R_{thJL})

The purpose of this test is to determine the power-handling capability of an ABD, at a given reference temperature. The thermal resistance of a semiconductor device is a measure of the ability of its mechanical structure to provide for heat removal from the active semiconductor element. (See MIL-STD-750 method 3101 or 4081). Thermal resistance, R_{thJR}, is the limiting value of thermal impedance, Z_{thJR}, at long time duration, t. The testing is the same as for thermal impedance, with the additional requirement that thermal equilibrium must occur by the end of the heating power pulse. See thermal impedance testing in 4.7 for further details.

4.9 Peak ESD limiting voltage (V_P) or clamping voltage (V_C or V_{CF})

The purpose of this test is to measure the peak voltage (V_P) [or the clamping voltage (V_C)] such as experienced during an electrostatic discharge (ESD) impulse. Typically a contact-mode human body model (HBM) ESD pulse similar to the IEC 1000-4-2 may be used for this test, but other standard or custom generator circuits may be used.

4.9.1 Procedure

Mount the ABD on a special designed two-layer printed circuit board (PCB) having a solid conducting surface on the opposite side of the components to be measured. A BNC connector shall be mounted on the solid conducting surface for attachment to an oscilloscope. A test point, for discharging an ESD generator, shall be located on the surface of the PCB with the ABD under test. The test circuit used shall be functionally equivalent to Figure 15. It is recommended that the oscilloscope have a bandwidth that is at least 1 GHz and an adequate sampling rate (e.g. 20 GS/s) in order to capture the signal shape. The Peak Voltage (*Vp*) and Clamping Voltage (*Vc*) are measured from the oscilloscope, as shown in Figure 16.

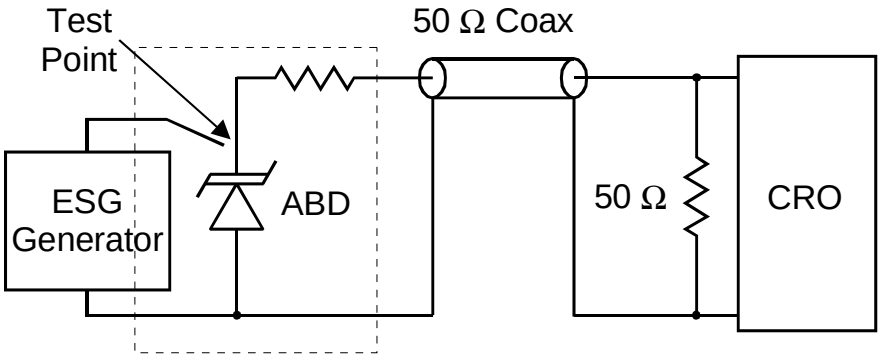


Figure 15 — ESD Peak voltage and clamp voltage test circuit

4.9.1 Procedure (cont'd)

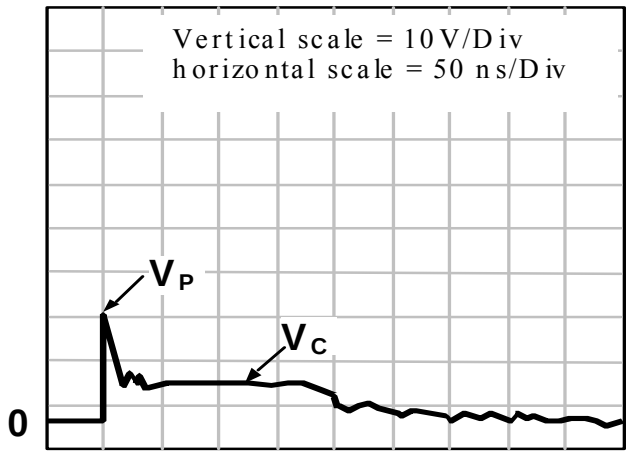


Figure 16 — Typical ABD peak and clamping ESD waveform

4.9.2 Test conditions to be specified

a. ESD generator voltage = _____ kV

b. Limiting (series) resistor (optional) = _____ Ω

c. ESD standard (if applicable) =_____

d. ESD generator resistance* = _____Ω

e. ESD generator capacitance* = _____pF

*required if ESD standard is not given

4.9.3 Characteristics to be measured

a. Peak voltage (V_P) = _____ V

b. Clamping voltage (V_C) = _____V

4.10 Crosstalk voltage (V_{CT})

The purpose of this test is to determine the voltage level coupled between adjacent multiple diode junctions (either discrete or monolithic structure) within a single package. This crosstalk voltage (V_{CT}) is the peak voltage measured across an ABD under test due to induced radiated effects between adjacent leads or temperature effects between adjacent junctions.

4.10.1 Procedure

Adjust the pulse generator to a voltage level equal to or less than the stand-off voltage (V_{WM}) of the ABD and a pulse width between 1 ns and 1 µs. With a dual-trace oscilloscope, monitor the rise and fall times of the test pulse. Measure the peak crosstalk voltage across the adjacent ABD within the packaged array. The test circuit used shall be functionally equivalent to Figure 17.

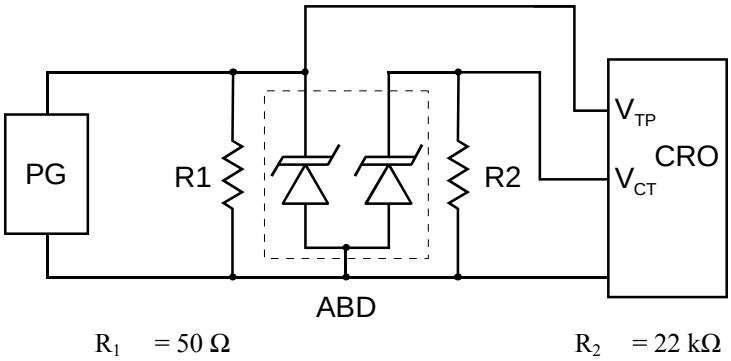


Figure 17 — Crosstalk voltage test circuit

4.10.2 Test conditions to be specified

a. Voltage test pulse (V_{TP}) = _____ V

b. Pulse width (t_d) = _____ ns

c. Rise time (t_r) of the pulse = _____ ns

d. Fall time (t_f) of the pulse = _____ ns

4.10.3 Characteristics to be measured

a. Peak Crosstalk voltage (V_{CT}) = _____ V

4.11 Signal line balance

4.11.1 Test description

This test is used to determine the level of line unbalance caused by a protective component. The differential-to-common mode voltage balance is the ratio of v_d, the differential mode voltage across the line termination, to v_c, the common mode voltage between the line termination and ground. It is expressed as a differential-to-common mode voltage balance coefficient, $BALANCE_{d\text{-}c}$, in dB, which is given by:

$$BALANCE_{d\text{-}c} = 20\log_{10}(v_d / v_c) \quad \text{dB}$$

The protective network is tested in a system consisting of a source, interconnecting line and a termination. The source shall be balanced to the ground plane in ac voltage and impedance. In some cases the source may supply a dc voltage component. The source values shall be the same as the intended application values. Where the ac component is digital, a squarewave source voltage shall be used having the same peak-to-peak voltage value as the digital signal and at a frequency equal to the highest digital rate (shown with a dotted lined connection). The termination load shall be the same impedance value as the line. Specific applications may also require the use of the transmission cable or a loop simulator to be used between the source and line termination. The measurements shall be made at a sufficient number of spot frequencies to characterize the component over the required frequency range.

Without the protective circuitry, a balanced line shall be set up. Any residual unbalance shall be adjusted to be at least 20 dB lower than the expected value with the protector in circuit or the required minimum balance standard, which ever is the more demanding. The protective circuitry is then connected to the line immediately before the termination and, if required, to the ground plane. The levels of common mode and differential mode voltage are then measured with equipment that does not change the voltage values by more than the intended measurement accuracy.

4.11.2 Test circuit

The test circuit is shown in Figure 18a and Figure 18b. A 2:1:1 ratio transformer, TX, converts the unbalanced oscillator signal into a balanced signal. The transformer shall not introduce a loss or distortion, which will affect the measurement accuracy. The oscillator's output impedance, R1, shall not be greater than the line impedance, Z_0 at the operating frequency. Resistor R2 is used to increase the source impedance such that $R1 + R2 = Z_0$. Capacitor C1 decouples the interconnection of the two secondary windings, its value is such that it does not develop any appreciable ac voltage component. DC voltage sources, PS1 and PS2, provide the required line dc bias conditions. For systems without dc bias capacitor C1 is removed and the power supplies, PS1 and PS2 are replaced by short circuits. Variable capacitors, C2 and C3, are used to balance the line for high frequency operation (without the protective circuit in place).

4.11.2 Test circuit (cont'd)

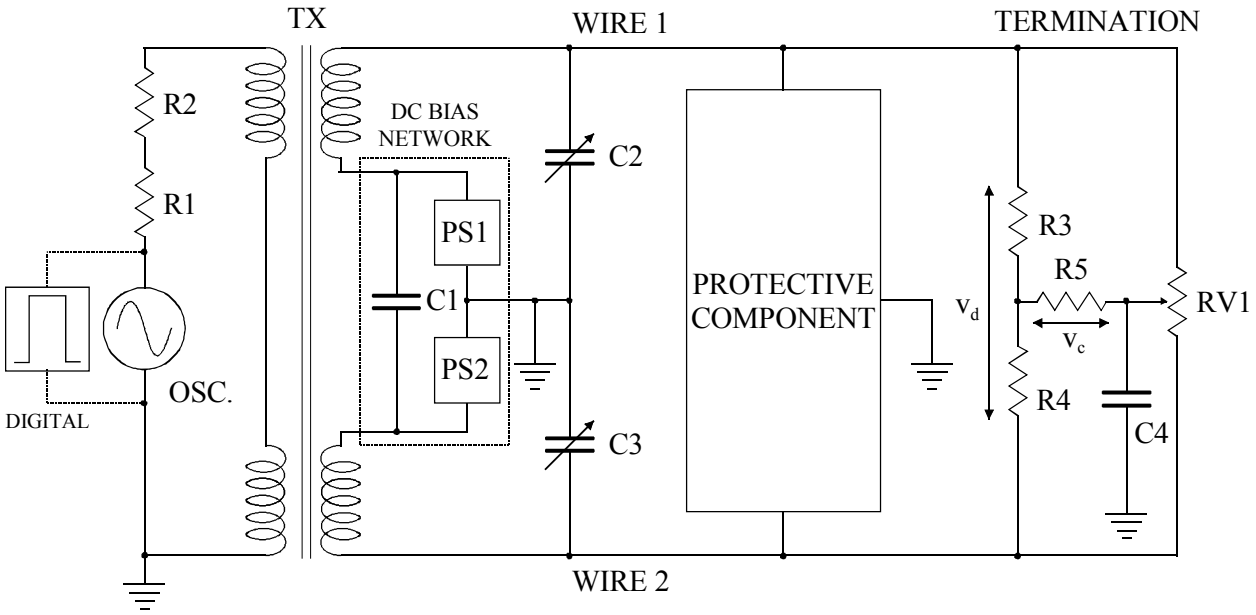


Figure 18a) — Line balance test circuit for three terminal protective components

The termination consists of two resistors, R3 and R4, with values such that R3 = R4 = $Z_0/2$. In conjunction with capacitor C4, resistor R5 provides a ground plane return for the junction of resistors R3 and R4. The value of resistor R 5 is such that R5 = $Z_0/2$. The value of capacitor C3 is such that it does not develop any appreciable ac voltage component. Potentiometer VR1 is used to balance the line for low frequency operation (without the protective circuit in place). The value of RV1 should not be less than 500 Z_0.

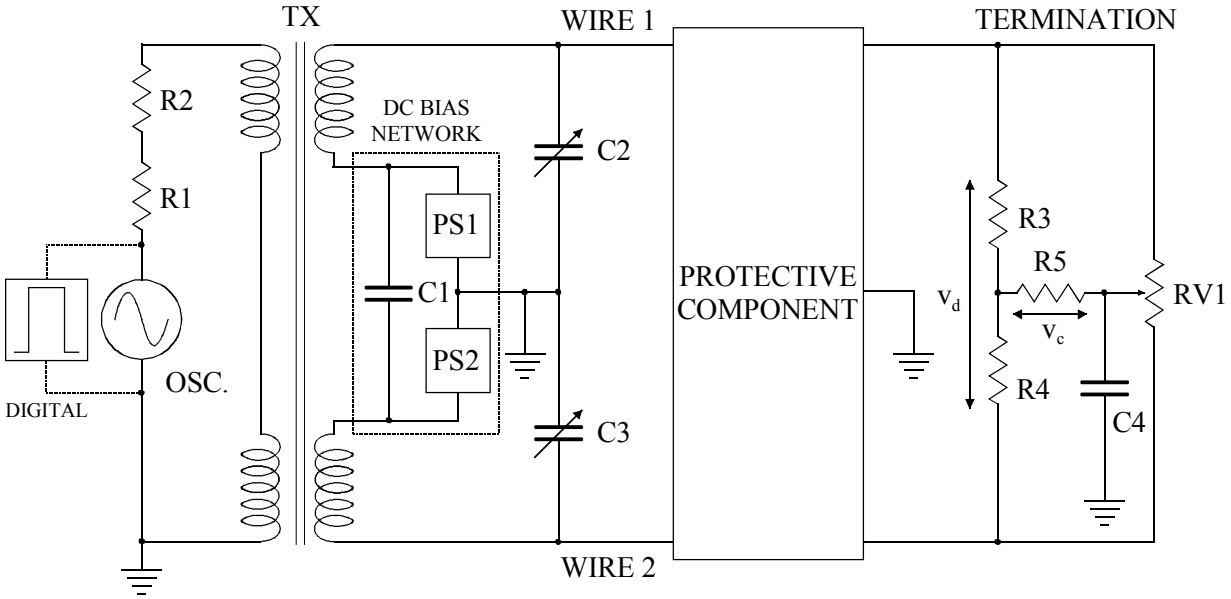


Figure 18b) — Line balance test circuit for five terminal protective components

4.11.2 Test circuit (cont'd)

The differential mode line voltage, v_d, is measured across the termination resistors R3 and R4. The common mode voltage, v_c, is measured across resistor R5. Other means (e.g. gain-phase analyzer) may be used to determine the balance coefficient specified herein, provided that there is adequate documentation of the appropriateness, precision and accuracy of the alternative measurement method.

4.11.3 Test conditions to be specified

a. Characteristic line impedance (Z_0) = _____Ω

b. Peak-to-peak ac voltage (v_d) = _____ V

c. Peak-to-peak as frequency (f) = ____ MHz

d. DC voltage on wire 1 (V_1) = ____ V

e. DC voltage on wire 2 (V_2) = ____ V

4.11.4 Characteristic to be measured

a. Peak-to-peak common mode termination voltage (v_c) = ____ V

4.11.5 Characteristic to be calculated

a. Differential-to-common voltage balance coefficient ($BALANCE_{d\text{-}c}$) = ____ dB
($BALANCE_{d\text{-}c} = 20\log_{10}(v_d/v_c)$ dB)

4.12 Simultaneous Surge

The purpose of this test is to duplicate worst-case simultaneous surges on ABDs that are configured with multiple protection lines in an array configuration. This may be of concern where the array is of a single monolithic structure rather than individual discrete elements or where a common-current path occurs by design or a common ABD element may occur for multiple lines exposed to a simultaneous surge.

NOTE This can occur for monolithic ABD arrays or other discrete arrays not electrically separated such as those with common ground lines or designs with other common active elements in a return current path during surges. Performance of simultaneous surges is used to determine vulnerability or performance level of those sensitive designs where current crowding effects may limit or derate the TVS array capability from that otherwise specified for each line when performed individually.

4.12.1 Procedure

Each intended surge line path of the ABD array shall be connected to a generator so that all can simultaneously be tested to the desired surge condition. The test circuit for achieving simultaneous surges on multiple lines is exemplified in Figure 19. The generated surge current in each line may also be determined by the individual resistor values shown. This method is to simulate the surge current or power rating otherwise provided to each line of the TVS array. If each of the multiple lines of the ABD is rated equally in surge current and clamping voltage, a single surge generator with a capacitive discharge principle may be used for a simultaneous surge as shown in Figure 18 using identical resistor values. If each line has a different surge current value or rating intended for this test, separate surge generators or resistor values may need to be connected to each line and synchronized in such a manner that all surges are triggered simultaneously.

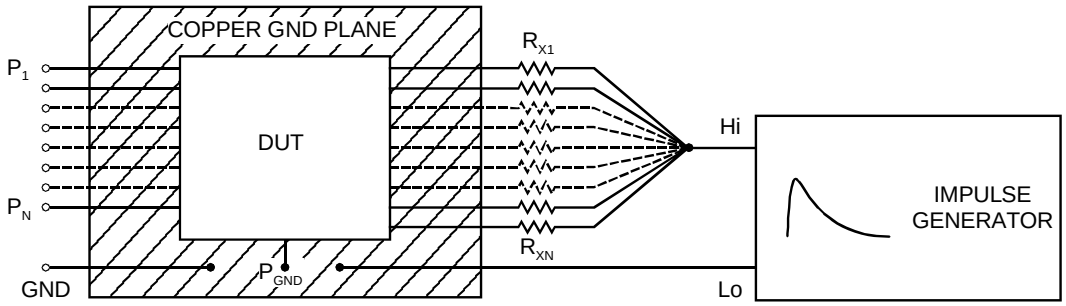


Figure 19 — Simultaneous surge test circuit

4.12.2 Test conditions to be specified

The "simultaneous surge test" is performed in a manner where each individual line is imposed with a desired Peak Pulse Current (I_{PP}) and specified waveshape at the same time to determine performance. Where applicable, it may also be used to characterize derating of ABD arrays for simultaneous surge conditions.

a. Ambient (T_A), case (T_C), or lead (T_L) temperature = _____ °C

b. Peak Pulse Current (I_{PP}) = _____ A

c. Waveshape = _____ /_____ µs

4.12.3 Characteristics to be measured

a. Clamping voltage (V_C) = _____ V

NOTE The clamping voltage for individual surges often specified for arrays may not apply for simultaneous surges where a common TVS element occurs for *all* multiple lines. After simultaneous surge testing of all protection lines of the DUT, the device may also require further testing for its other specified parameters to verify survival. As a minimum, this shall include standby current I_D at rated working standoff voltage V_{WM} for each applicable line and specified polarity.

4.13 Peak Overshoot Voltage (V_{OS})

The purpose of this test is to determine the overshoot voltage of the ABD during the testing of the clamping voltage.

4.13.1 Procedure

This test is the same as for the clamping voltage test in 4.3.1. During the clamping voltage test, the peak overshoot voltage V_{OS} is defined as that voltage above the clamping voltage, $V_P - V_C$. This is primarily due to parasitic inductive effects from fast-rise-time impulses. The test time for this measurement is greater than or equal to the pulse duration of the test waveform.

NOTE To assure that the peak overshoot voltage represents the ABD; all wires to the equipment and the ABD test leads are to be kept at minimum lengths. Also the test fixture for the measurement may be temporarily shorted and measured for peak overshoot voltage contribution for reference to subtract from the ABD reading of V_{OS}. The peak overshoot voltage is characteristic of the front time and the lead inductance of the ABD.

4.13.2 Test conditions to be specified

a. Ambient (T_A), case (T_C), or lead (T_L) temperature = _____ ^{o}C

b. Peak Pulse Current (I_{PP}) = _____ A

c. Waveshape = _____ /_____ µs

4.13.3 Characteristic to be calculated

a. Peak Overshoot Voltage (V_{OS}) = _____V

4.14 Temperature derating test method for I_{PPSM} or P_{PPSM}

The purpose of this test is to verify a derated I_{PPSM} or P_{PPSM} value at an elevated base temperate.

4.14.1 Procedure

a) Place the device under test in the middle of the oven with all necessary wiring connections secured for the surge test. Set the oven temperature to the desired elevated base temperature and allow the device to reach thermal equilibrium. Thermal equilibrium may be verified by taking consecutive measurements of a temperature sensitive characteristic, such as $V_{(BR)}$, at 5 minute intervals. When consecutive values differ by less than the equipment measurement accuracy, thermal equilibrium has been reached.

b) To verify the derated I_{PPSM} value, apply 10 pulses of the derated I_{PPSM} waveform with an interval between each pulse application that is sufficient to ensure thermal equilibrium. Typically this would require an interval of 30 seconds minimum. After testing and cooling to room ambient, the ABD shall not have any degradation or catastrophic fault modes.

c) To verify the derated P_{PPSM} value, the test must apply sufficient I_{PP} to make the multiplied product of the measured V_C and applied I_{PP} equal to the derated P_{PPSM} value. For linear I_{PPSM} derating to T_{JM}, the maximum possible I_{PP} value, I_{PPX}, at an elevated temperature T_X would be I_{PPSM} multiplied by the temperature difference of T_{JP} and the desired lead, case or ambient temperature T_X divided by the temperature difference of T_{JP} and the referenced 25 ^{o}C temperature: $I_{PPX} = I_{PPSM}\,(T_{JP} - T_X)/(T_{JP} - 25\ ^{o}\text{C})$. The lead, case or ambient temperature T_X cannot exceed the TJM value. To allow a safety margin, the first applied impulse should be 0.5 I_{PPX} for measuring the value of VC. Based on the calculated I_{PPVC} value, the applied value of I_{PP} shall be progressively increased on subsequent impulse until the derated value of P_{PPM} is reached. A further nine pulses of the derated value of P_{PPM} are then applied to the ABD with a 30 second minimum interval between each. After testing and cooling to room ambient, the ABD shall not have any degradation or catastrophic fault modes.

Annex A (informative) Differences between revisions

This table briefly describes most of the changes made to entries that appear in this standard, JESD210A, compared to its predecessor, JESD210 (December 2007). If the change to a concept involves any words added or deleted (excluding deletion of accidentally repeated words), it is included. Some punctuation changes are not included.

Clause	Description of change
2.3.2.2	**Note 1,** Added sentence to give more detail about graphical derating.
2.3.2.2	**Note 2,** Added words "stead-state".
2.3.2.2	**Note 3,** Rewrote note to better explain difference between stead-state and peakpulse deratings.
2.3.2.2	**Note 4,** Added note to explain how the average power-derating curve is derived.
2.3.2.2	**Note 5,** Added note to explain how the peak-pulse power-derating curve is derived.
2.3.2.2	**Note 6 & Figure 7,** Added figure showing typical derating curve for P_{PPSM} and $P_{M(AV)}$.
4.14	Added temperature derating test method for I_{PPM} or P_{PPM}.

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1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

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2. Recommendations for correction:

_____

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